Abstract

A circuit to divide down the frequency of a clock signal, where embodiment circuits comprise a set-reset flip-flop feeding its output to a shift register, and combinational logic to provide feedback from the shift register to the set input port, reset input port, or both set and reset input ports of the set-reset flip-flop. The set-reset flip-flop and shift register are clocked by the clock signal. The output signal of the circuit may be taken at any output port of the shift register or the set-reset flip-flop. In one embodiment, the state of the shift register is represented by the set of Boolean values Q<i>, i = 1, 2, ..., N-1, and the combinational logic provides to the set input port of the set-reset flip-flop the Boolean value $\{Q^{\#}<M-1> \wedge <Q^{\#}<M-2> \wedge \ldots \wedge Q^{\#}<0>\}$, where $Q^{\#}<i>$ is the Boolean complement of Q<i>, $Q^{\#}<0>$ is provided by the set-reset flip-flop, $\wedge$ is Boolean AND, and M is a positive integer not greater than N; and the combinational logic also provides the Boolean value $\{Q<L-1> \wedge <Q<L-2> \wedge \ldots \wedge Q<0>\}$ to the reset input port of the set-reset flip-flop, where L is a positive integer not greater than N. For such an embodiment, the frequency of the output signal is that of the clock signal divided down by the divisor D where D = L + M, and the duty cycle of the output signal is L/D.